Claim 1, which has been amended merely to more specifically claim the invention, recites:

> "A computer-implemented method for remapping between pixel coordinate space and memory address space, comprising the steps of:
>
> a) defining a phantom port containing a plurality of sequential memory addresses;
>
> b) generating an address to the phantom port using a conventional addressing scheme;
>
> c) determining an address in memory address space corresponding to the generated phantom port address; and
>
> d) accessing the address in memory address space."

Claim 22, which has been amended merely to more specifically claim the invention, recites:

> "A system for remapping between pixel coordinate space and memory address space, comprising:
>
> a central processing unit;
>
> a frame buffer memory coupled to the central processing unit and having an associated memory address scheme;
>
> a memory address device coupled to the central processing unit for defining a phantom port containing a plurality of sequential memory addresses, each of a subset of the memory addresses mapping to an address in the frame buffer memory; and
>
> a remapping device coupled to the memory address device for converting an address between the memory address scheme of the frame buffer memory and a memory address of the phantom port."

As discussed in the specification as originally filed, the use of the phantom port provides distinct advantages over the prior art. In particular, the phantom port performs remapping without requiring expensive multiply or divide operations. Thus, the use of a phantom port yields improved performance over remapping techniques employed by the prior art, and thereby facilitates more efficient graphics operations.

By contrast, none of the cited references teaches or discloses the use of a phantom port as claimed herein. Nagashima merely discloses a texture address generator, texture pattern generator, texture drawing device, and texture address generating method. The portion of Nagashima cited by the Examiner

(col. 9, lines 9-12) merely discloses that texture data is read out based on a one-dimensional address that is obtained by a two-dimensional address converter. Address conversion from two dimensions to one dimension as described by Nagashima is well known in the art, and in fact was described in the Description of the Related Art of the present application. However, there is no hint or suggestion in Nagashima of the use of a phantom port as claimed herein.

Wilde merely discloses a graphics subsystem which stores graphics texture maps internal to a graphics processor to enable fast storage and retrieval to a graphics drawing engine. The Examiner cited col. 5, lines 54-59, which merely describe a tiled memory format for texture storage in display memory, and a tile linear format for texture storage in host system memory. The Examiner stated that an address converter in inherent in view of the different formats. However, there is no hint or suggestion in the disclosure of Wilde, of any technique or system for remapping between pixel coordinate space and memory address space using a phantom port, as claimed herein.

Wang et al. merely discloses an address converter for performing two-dimensional virtual coordinate to linear physical memory address conversion. The system described by Wang et al. operates in an entirely different manner than the system and method claimed herein. In particular, Wang et al. employs an edge walking circuit, span expansion circuit, and linear address circuit which operate to generate two-dimensional virtual coordinates, selectively expand the coordinates according to the number of bits used and the amount of information which can be accessed at a time from memory, and outputting a linear physical address. There is no hint or suggestion of any technique or system for remapping between pixel coordinate space and memory address space using a phantom port, as claimed herein.

The Examiner stated that the phantom port of the present invention is nothing more than an address converter of prior art. Applicant respectfully disagrees. As described in the specification, the phantom port contains a plurality of memory addresses, and operates to accept conventional linear addresses from the CPU and remap them into tiled addresses for accessing frame buffer memory. By contrast, the cited art merely disclose various forms of generic address converters that convert two-dimensional addresses to one-dimensional addresses. Thus, the prior art would fail to achieve the distinct performance advantages of the present invention, which result from the use of the phantom port and the capability of improving efficiency of graphics operations that result therefrom. In particular, as described in the specification, the phantom port facilitates address conversion without the necessity for complex arithmetic operations.

Thus, although various forms of address conversion are contemplated by the prior art, none of these systems as described provides the performance advantages facilitated by the claimed limitations of the present invention.

Claims 2 through 5 are dependent upon claim 1, and incorporate all of the limitations of claim 1, including those that distinguish the claims from the cited references. Claim 23 is dependent upon claim 22, and incorporates all of the limitations of claim 22, including those that distinguish the claims from the cited references. Claims 2 through 5 and 23 further recite additional limitations.

In particular the limitation of claims 4 and 23 that "the phantom port has a span size equal to a power of two" provides further performance advantages by allowing remapping operations to be implemented using simple field extraction and bit shifting, as described in the specification. The Examiner stated that such a limitation would be obvious of, if not inherent to, due to

the teachings of Nagashima, Wilde, or Wang et al. because the size of the buffer is always equal to a power of two. However, Applicant can find no teaching or suggestion in any of the cited references of such a limitation. Furthermore, even if the cited references were modified to provide a buffer size with a power of two, such a modification would still fail to yield the claimed invention, since the claim is expressly limited to a phantom port having a span size equal to a power of two, which provides distinct performance advantages. Thus, a modified version of one of the cited references having a buffer size with a power of two would still fail to provide the performance advantages of the present invention as recited in claims 4 and 23.

Claim 5 recites a further limitation that "c) comprises determining an address in memory address space by extracting at least one field from the phantom port address." The determination of a memory address is thus performed in a highly efficient manner by simple extraction of a field, thereby further improving performance. Applicant can find no hint or suggestion in the teachings of Nagashima, Wilde, or Wang et al. of the use of field extraction as recited in claim 5. Thus, none of the cited references would provide the distinct performance advantages facilitated by the invention of claim 5.

Applicant respectfully submits that the limitations of claims 2-5 are not suggested nor made obvious by the cited references.

Claim 6 recites:

> "A computer-implemented method for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, the method comprising the steps of:
>
> a) determining a span of first coordinates of pixels of the display panel;
> b) defining a virtual frame buffer having a first dimension at least as large as the span of the first coordinates;
> c) generating a virtual address indicating a first coordinate and second coordinate of a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel, with the virtual address identifying a memory cell; and

d) performing one of a reading operation and a writing operation of a representation of the pixel in the memory cell identified by the virtual address."

Claim 14 recites:

"A computer-implemented method for accessing representations of pixels of a display panel in a frame buffer, the display panel having a plurality of pixels each pixel having a first coordinate and a second coordinate, the method comprising the steps of:

a) determining a span of first coordinates of pixels of the display panel;
b) selecting a second tile span representing a length of a tile of the display panel along the second coordinates of pixels of the display panel;
c) defining a virtual frame buffer having a first dimension at least as large as the span of the first coordinates times the second tile span;
d) generating a virtual address indicating a first coordinate and a second coordinate for a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel; and
e) performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell of the frame buffer identified by the virtual address."

Claim 24 recites:

"A system for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, comprising:

a processing unit;
a data accessing module for converting pixel coordinates to virtual frame buffer addresses;
a video controller for transmitting video data;
a system memory including a frame buffer for storing digital video data;
a bus coupled to the processing unit, the data accessing module, the video controller, and the system memory, for transmitting data therebetween; and
a display system coupled to the video controller for receiving and displaying video data on the display panel."

The claimed method and system thus employ a virtual frame buffer to provide rapid addressing of video data. A virtual address for a pixel can be rapidly generated by the present invention using shifting, replacing, or concatenation operations applied to received coordinates of a pixel without the need for the complicated and relatively slow arithmetic hardware. The present invention can access the frame buffer quickly using the virtual address for reading or writing video data in the associated memory cell of the frame

buffer. Expensive multiply and divide operations are avoided in favor of concatenation, shifting, and simple field extraction, as described in the specification.

None of the cited references discloses any technique resembling the claimed method. As discussed above, the cited portions of Nagashima, Wilde, and Wang et al. merely disclose or hint at various address conversion techniques. However, Applicant can find no suggestion in the cited art of defining a virtual frame buffer and generating a virtual address associated therewith, as claimed herein. Thus, the cited art would still fail to yield the performance advantages facilitated by the virtual frame buffer and virtual addresses as claimed herein.

Claims 7 through 13 are dependent upon claim 6, and incorporate all of the limitations of claim 6, including those that distinguish the claims from the references. Claims 15 through 17 and 19 through 21 are dependent upon claim 14, and incorporate all of the limitations of claim 14, including those that distinguish the claims from the references. Claims 25 through 29 are dependent upon claim 24, and incorporate all of the limitations of claim 24, including those that distinguish the claims from the references. Claims 7-13, 15-17, 19-21, and 25-29 further recite additional limitations. In particular, claims 8 and 16 recite "defining a base value, and wherein the first dimension of the virtual frame buffer is a power of the base value." This provides additional performance benefits by allowing remapping to occur using simple shifting and extraction operations. Claim 10 recites "concatenating the bit representation of the first coordinate of the pixel to the bit representation of the second coordinate of the pixel." The recited limitation thus provides another technique for improving performance in remapping using simple concatenation operations and avoiding expensive addition or multiplication operations.

Applicant respectfully submits that such limitations are not suggested nor made obvious by the cited references. If the Examiner disagrees, Applicant respectfully requests that the Examiner point out where in the disclosures of the cited references such a technique is taught.

In addition, claim 26 recites that "the virtual frame buffer addresses are arranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses using concatenation." Claim 27 recites that "the first and second coordinates of the pixel are stored as bit representations and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses by concatenating the bit representation of the first coordinate of the pixel to the bit representation of the second coordinate of the pixel." These limitations facilitate improved performance by allowing pixel coordinates to be converted using simple concatenation, without the need for more complex mathematical operations. Claim 29 recites that "the virtual frame buffer addresses are arranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts virtual frame buffer addresses to pixel coordinates using bit field extraction." This limitation facilitates improved performance by allowing pixel coordinates to be converted using simple bit field extraction. Applicant respectfully submits that such limitations are not suggested nor made obvious by the disclosures of the cited references, which merely mention or hint at address conversion.

Accordingly, Applicants respectfully submit that claims 1-29 are patentable over the cited art.

No additional fee is due.

On the basis of the above amendments and remarks, consideration of this application and the early allowance of all claims herein are requested.

Favorable action is solicited.

Respectfully submitted,

ROGER W. SWANSON

Dated: APR 29/99 By: _____

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